

## WHAT IS CLAIMED IS:

1. A method for providing a bi-directional communication bus between a first  
2 processing unit (PU) and a second and third PU each adjacent to the first PU and  
3 within M processing units (PUs), wherein the first PU is physically coupled to the  
4 second PU with a first Link input and a first Link output and to the third PU with a  
5 second Link input and a second Link output, the method comprising the steps of:

6 sending a first output signal from an output of the first PU to the third PU on  
7 the second Link output or selectively sending a second output signal received on the  
8 first Link input from the second PU to the third PU on the second Link output in  
9 response to the first logic state of a first enable signal;

10 selectively sending a third output signal received on the second Link input  
11 from the third PU or the first output signal from the first PU to the second PU on the  
12 first Link output in response to the first logic state of a second enable signal; and

13 receiving, in an input of the first PU, the third output signal received on the  
14 second Link input from the third PU or selectively receiving the second output signal  
15 on the first Link input from the second PU when the first enable signal has the first  
16 logic state.

1. 2. The method of claim 1, wherein the first and second enable signals are  
2 generated by control logic in the first PU.

1. 3. The method of claim 1, wherein communication between the second PU and  
2 the first and third PU is blocked when the first and second enable signals concurrently  
3 are at a second logic state.

1       4.     The method of claim 1, wherein the second PU has a second Link output  
2     coupled to the first Link input of the first PU and a second Link input coupled to the  
3     first Link output of the first PU.

1       5.     The method of claim 1, wherein the third PU has a first Link input coupled to  
2     the second Link output of the first PU and a first Link output coupled to the second  
3     Link input of the first PU.

1       6. A bi-directional communication bus in each of M processing units (PUs) for  
2 bi-directional communication between a first processing unit (PU) and a second and  
3 third PU each adjacent to the first PU and within the M PUs, wherein the first PU is  
4 physically coupled to the second PU with a first Link input and a first Link output and  
5 to the third PU with a second Link input and a second Link output comprising:

6           circuitry for coupling a first output signal from an output of the first PU to the  
7 third PU on the second Link output or selectively coupling a second output signal  
8 received on the first Link input from the second PU to the third PU on the second  
9 Link output in response to the first logic state of a first enable signal;

10           circuitry for selectively coupling a third output signal received on the second  
11 Link input from the third PU or the first output signal from the first PU to the second  
12 PU on the first Link output in response to the first logic state of a second enable  
13 signal; and

14           circuitry for coupling the third output signal received on the second Link to an  
15 input of the first PU or selectively coupling the second output signal on the first Link  
16 input from the second PU when the first enable signal has the first logic state.

1       7. The bi-directional bus of claim 6, wherein the first Link input and a first  
2 function output from function logic circuitry are coupled to communication logic  
3 circuitry generating a first function output signal on the first Link output and a first  
4 communication output signal on a first communication output.

1       8. The bi-directional bus of claim 7, wherein the second Link input and the first  
2 communication output are coupled to the function logic circuitry generating a second  
3 function output signal on the first Link output and a second function output signal on  
4 a first function output.

1       9.     The bi-directional bus of claim 8, wherein the first communication output  
2     signal is generated as a logic combination of the second output signal from the second  
3     PU and the first enable signal in a first logic gate.

1       10.    The bi-directional bus of claim 9, wherein the first function output signal is  
2     generated as a logic combination of the second function signal and the second enable  
3     signal in a second logic gate.

1       11.    The bi-directional bus of claim 10, wherein the second function signal is  
2     generated as a logic combination of the first communication signal and the first  
3     output signal in a third logic gate.

1       12.    The bi-directional bus of claim 11, wherein the second function signal is  
2     generated as the logic combination of the second function signal and the third output  
3     signal in a fourth logic gate.

1       13.    The bi-directional bus of claim 7, wherein the input of the first PU is coupled  
2     to the first function output of the function logic circuit.

1       14.    The bi-directional bus of claim 12, wherein the first and second logic gates are  
2     AND logic gates.

1       15.    The bi-directional bus of claim 12, wherein the third and fourth logic gates are  
2     OR logic gates.

1       16. The bi-directional bus of claim 6, wherein bi-directional communication  
2       between the first and second PU are enabled by setting both the first and second  
3       enable signals to a logic one.

1       17. The bi-directional bus of claim 6, wherein the first and second PUs are pattern  
2       detection processing units, each for comparing an input data byte to a pattern byte  
3       selected for a sequence of pattern bytes stored in each of the first and second PUs and  
4       generating a compare output in each of the first and second PUs, wherein the pattern  
5       byte in each of the PUs is selected by an address pointer and modified in response to  
6       a logic state of the compare output and an operation code stored with the selected  
7       pattern byte.

1       18. The bi-directional bus of claim 17, wherein the bi-directional communication  
2       between the first PU and the second PU is enabled to allow increment signals from  
3       the first and second PU, for incrementing their respective address pointers, to be  
4       coupled to and logic combined in the control logic of the first PU and control logic of  
5       the second PUs to generate a modified increment address pointer signal at the PU  
6       input of the first PU and the one or more adjacent PUs.

1       19. The bi-directional bus of claim 18, wherein the modified increment address  
2       pointer signal is used to enable advanced matching capabilities to be performed by  
3       the first and second PU by incrementing the address pointer in the first PU or the  
4       second PU if either the first or second PU generates a logic state on its corresponding  
5       compare output indicating that a particular input data byte has compared to either  
6       selected pattern byte in the first or second PU.

1       20. A data processing system comprising:

2           a central processing unit (CPU);

3           a random access memory (RAM);

4           one or more parallel pattern detection engines (PPDEs);

5           a bus coupling the CPU, RAM, and the one or more PPDEs, wherein each of

6       the PPDEs has an input/output (I/O) interface for coupling data into and out of the

7       PPDEs, M pattern detection processing units (PUs), and a cascade system for

8       providing a bi-directional communication bus circuitry in each of M PUs for bi-

9       directional communication between a first processing unit (PU) and a second and

10      third PU each adjacent to the first PU and within the M PUs, wherein the first PU is

11      physically coupled to the second PU with a first Link input and a first Link output and

12      to the third PU with a second Link input and a second Link output comprising:

13           circuitry for coupling a first output signal from an output of the first PU to the

14       third PU on the second Link output or selectively coupling a second output signal

15       received on the first Link input from the second PU to the third PU on the second

16       Link output in response to the first logic state of a first enable signal;

17           circuitry for selectively coupling a third output signal received on the second

18       Link input from the third PU or the first output signal from the first PU to the second

19       PU on the first Link output in response to the first logic state of a second enable

20       signal; and

21           circuitry for coupling the third output signal received on the second Link to an

22       input of the first PU or selectively coupling the second output signal on the first Link

23       input from the second PU when the first enable signal has the first logic state.

1       21. The data processing system of claim 20, wherein the first Link input and a

2       first function output from function logic circuitry are coupled to communication logic

3       circuitry generating a first function output signal on the first Link output and a first  
4       communication output signal on a first communication output.

1       22.    The data processing system of claim 21, wherein the second Link input and  
2       the first communication output are coupled the function logic circuitry generating a  
3       second function output signal on the first Link output and a second function output  
4       signal on a first function output.

5       23.    The data processing system of claim 22, wherein the first communication  
6       output signal is generated as a logic combination of the second output signal from the  
7       second PU and the first enable signal in a first logic gate.

8       24.    The data processing system of claim 23, wherein the first function output  
9       signal is generated as a logic combination of the second function signal the and the  
10      second enable signal in a second logic gate.

1       25.    The data processing system of claim 24, wherein the second function signal is  
2       generated as a logic combination of the first communication signal and the first  
3       output signal in a third logic gate.

1       26.    The data processing system of claim 25, wherein the second function signal is  
2       generated as the logic combination of the second function signal and the third output  
3       signal in a fourth logic gate.

1       27.    The data processing system of claim 21, wherein the input of the first PU is  
2       coupled to the first function output of the function logic circuit.

1       28. The data processing system of claim 26, wherein the first and second logic  
2       gates are AND logic gates.

1       29. The data processing system of claim 26, wherein the third and fourth logic  
2       gates are OR logic gates.

1       30. The data processing system of claim 20, wherein bi-directional  
2       communication between the first and second PU are enabled by setting both the first  
3       and second enable signals to a logic one.

1       31. The data processing system of claim 20, wherein the first and second PUs are  
2       pattern detection processing units, each for comparing an input data byte to a pattern  
3       byte selected for a sequence of pattern bytes stored in each of the first and second  
4       PUs and generating a compare output in each of the first and second PUs, wherein the  
5       pattern byte in each of the PUs is selected by an address pointer and modified in  
6       response to a logic state of the compare output and an operation code stored with the  
7       selected pattern byte.

1       32. The data processing system of claim 31, wherein the bi-directional  
2       communication between the first PU and the second PU is enabled to allow increment  
3       signals from the first and second PU, for incrementing their respective address  
4       pointers, to be coupled to and logic combined in the control logic of the first PU and  
5       control logic of the second PUs to generate a modified increment address pointer  
6       signal at the PU input of the first PU and the one or more adjacent PUs.

1       33. The data processing system of claim 32, wherein the modified increment  
2       address pointer signal is used to enable advanced matching capabilities to be

3       performed by the first and second PU by incrementing the address pointer in the first  
4       PU or the second PU if either the first or second PU generates a logic state on its  
5       corresponding compare output indicating that a particular input data byte has  
6       compared to either selected pattern byte in the first or second PU.

1       34. A processing unit (PU) bi-directional communication bus coupling a  
2       processing unit PU(N) and a first adjacent PU(N-1) and second adjacent PU(N+1)  
3       within a group of M PUs, wherein each PU(N) has a bus circuit (BC) and a BC(N) in  
4       PU(N) is physically coupled to a BC(N-1) in PU(N-1) with a first Link input and a  
5       first Link output and BC(N) is coupled to a BC(N+1) in PU(N+1) with a second Link  
6       input and a second Link output, wherein BC(N) comprises:

7               function logic receiving a PU output signal PUO(N) from P(N), a first gated  
8       communication signal (GCS1) from PU(N-1), and a first communication signal (CS1)  
9       from PU(N+1) on the second Link input and generating a second communication  
10      signal (CS2) on the second Link output and a second gated communication signal  
11      (GCS2), wherein CS2 is a logic combination of the PUO(N) and GCS1 and GCS2 is a  
12      first logic combination of the CS1 and CS2; and

13               communication logic receiving a third communication signal (GS3) from the  
14       PU(N-1) and GCS2 and generating a fourth communication signal (GS4) on the first  
15       Link output and generating GCS1, wherein CS4 is a second logic combination of  
16       GCS2 and a logic state of a chain out signal and GCS1 is a logic combination of CS3  
17       and a first chain in signal and wherein GCS2 is coupled to the PU(N) as a first PU  
18       input signal PUI(N).

1       35. The bi-directional bus of claim 12, wherein CS4 is generated as a logic AND  
2       combination of GCS2 and a logic state of the chain out signal and GCS1 is generated  
3       as a logic AND combination of CS3 and a logic state of the chain in signal.

1       36. The bi-directional bus of claim 12 wherein CS2 is generated as a logic OR  
2       combination of GCS1 and PUO(N) and GCS2 is generated as a logic OR combination  
3       of CS2 and CS1.

1       37.    The bi-directional bus of claim 6, wherein GCS2 is coupled as an input signal  
2       to PU(N).

1       38.    The bi-directional bus of claim 6, wherein the M PUs are pattern detection  
2       processing units, each for comparing input data to selected pattern data from pattern  
3       data stored in each of the M PUs and generating a compare output in each of the M  
4       PUs, wherein the selected pattern data in each of the M PUs is selected by an address  
5       pointer that is modified in response to a logic state of the compare output and an  
6       operation code stored with the selected pattern data.